High-performance polycrystalline silicon thin-film transistors integrating sputtered aluminum-oxide gate dielectric with bridged-grain active channel

2013 Semicond. Sci. Technol. 28 115003

(http://iopscience.iop.org/0268-1242/28/11/115003)

Semicond. Sci. Technol. **28** (2013) 115003 (5pp) doi:10.1088/0268-1242/28/11/115003

High-performance polycrystalline silicon thin-film transistors integrating sputtered aluminum-oxide gate dielectric with bridged-grain active channel

Meng Zhang[1], **Wei Zhou, Rongsheng Chen, Man Wong and Hoi-Sing Kwok**

Center for Display Research and Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong

E-mail: zhangmeng@ust.hk

Received 30 May 2013, in final form 31 July 2013
Published 18 September 2013
Online at stacks.iop.org/SST/28/115003

Abstract

Polycrystalline silicon thin-film transistors (TFTs) integrating sputtered Al_2O_3 gate dielectric with bridged-grain active channel are demonstrated. The proposed TFTs exhibit excellent device performance in terms of smaller threshold voltage, steeper subthreshold swing and higher on-current/off-current ratio. More importantly, the mobility of the proposed TFT is 5.5 times that of conventional TFTs with SiO_2 gate dielectric. All of these results suggest that the proposed TFT is a good choice for low-power and high-speed driving circuits in display application.

(Some figures may appear in colour only in the online journal)

1. Introduction

Polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have received considerable research interest due to their high carrier mobility, which could provide possible solutions for the integration of peripheral circuit and active matrix in display applications [1]. High-performance poly-Si TFTs with low operating voltage, steep subthreshold swing (*SS*) and large on-current/off-current (I_{on}/I_{off}) ratio are thus desired to accomplish the low-power and high-speed display driving circuits. However, poly-Si thin films, especially for solid-phase-crystallized (SPC) film, have numerous grain boundaries (GBs) inside [2, 3], resulting in large threshold voltage (V_{th}), poor *SS* and small I_{on}/I_{off} ratio in poly-Si TFTs. Scaling down the conventional gate dielectrics (i.e., SiO_2 or Si_3N_4) can increase gate capacitance and satisfy some demands listed above but would cause a higher gate-leakage current and bring more serious reliability issues due to the thinner oxide [4]. To maintain the physical gate dielectric thickness while increasing gate capacitance, several high-*k* gate dielectric materials [4–7], such as Al_2O_3 [4], HfO_2 [5], Pr_2O_3 [6] and Y_2O_3 [7], are applied into the poly-Si TFTs to improve device electrical characteristics. Nevertheless, poly-Si TFTs with high-*k* gate dielectrics suffer from a more undesirable gate-induced drain leakage (*GIDL*) current due to the larger permittivity of high-*k* gate dielectrics [4–12].

In this work, poly-Si TFTs integrating a high-*k* Al_2O_3 gate dielectric with bridged-grain (BG) [2] SPC active channel is first demonstrated. By employing Al_2O_3 gate dielectric and BG active channel, the SPC poly-Si TFTs exhibit outstanding electrical characteristics in terms of smaller V_{th}, steeper *SS*, larger I_{on}/I_{off} ratio and especially much lower *GIDL* current, compared to the control SPC TFTs. It is also worth mentioning that the maximum field-effect mobility (μ_{FE}) of proposed TFTs is up to 47.92 $cm^2\ Vs^{-1}$, which is 4.5 times larger than that of SPC poly-Si TFTs with low-pressure chemical vapor deposition (LPCVD) SiO_2 gate dielectric and 1.9 times larger than that of SPC poly-Si TFT with sputtered Al_2O_3 gate dielectric.

[1] Author to whom any correspondence should be addressed.

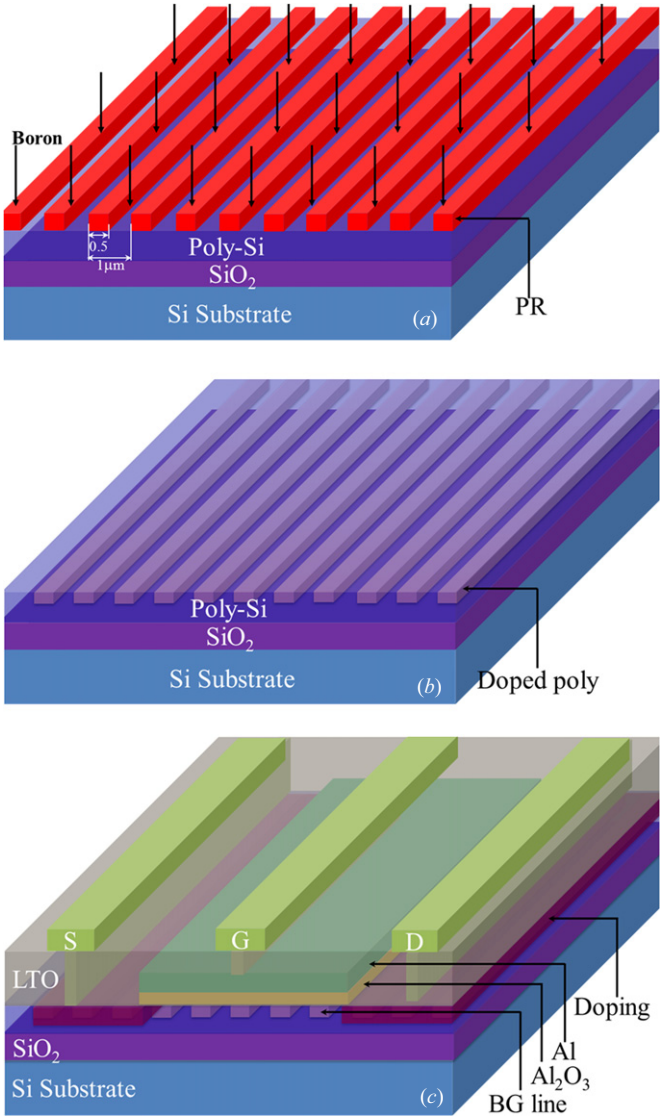

Figure 1. Schematic illustration of device fabrication process flow of BG SPC TFT with Al_2O_3. (*a*) Pattern formation of BG lines. The red cuboids stand for photoresist. (*b*) The schematic of active channel with selective boron doped BG lines. (*c*) Schematic of the proposed BG SPC TFTs with Al_2O_3 gate dielectric.

2. Experimental

TFTs used in this study were in conventional self-aligned top-gate structure. A schematic illustration of device fabrication process flow is shown in figure 1. First, a layer of 100-nm-thick amorphous-Si (a-Si) was deposited on an oxidized silicon wafer by LPCVD. Then the a-Si layer is crystallized by SPC method at 600 °C for 24 h in N_2 ambient. After crystallization, a layer of photoresist (PR) was coated on the wafer and then patterned into a series of lines as shown in figure 1(*a*). The red cuboids stand for remaining PR after photolithography. The scanning electron microscope (SEM) image and atomic force microscope (AFM) image of BG line pattern after lithography are shown in figures 2(*a*) and (*b*), respectively. It can be observed that the period of BG lines is about 1 μm and the PR-covered line ratio in one period is about 50%, as also shown in

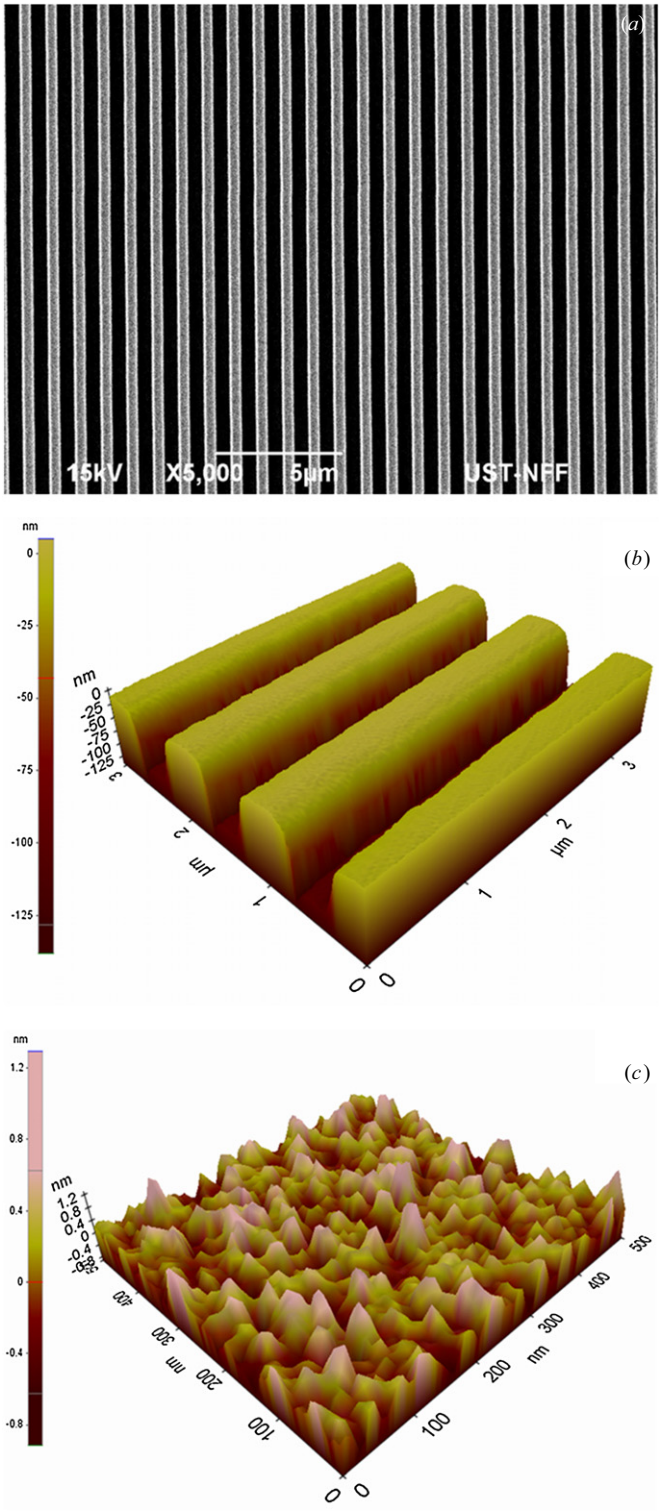

Figure 2. (*a*) SEM image and (*b*) AFM image of BG line pattern after lithography. (*c*) AFM image of the 70-nm-thick Al_2O_3 film sputtered on the bare Si wafer.

figure 1(*a*). Boron implantation with a dose of 10^{15} cm^{-2} was then performed. After the implantation, the PR is removed. Subsequently, the doped BG poly-Si lines inside the poly-Si thin film were formed as shown in figure 1(*b*). Then the active layer was defined and patterned by photolithography

and wet etching. Next, 70-nm-thick Al_2O_3 was deposited using reactive dc magnetron sputtering method in a mixed Ar and O_2 ambient at room temperature. The deposition pressure and the power were 3 mTorr and 120 W, respectively. The AFM image of the 70-nm-thick Al_2O_3 film sputtered on bare Si wafer is shown in figure 2(*c*). The root mean square surface roughness is 0.489 nm. The measured capacitance density of Si/53-nm-thick-Al_2O_3/Al capacitor with area of 50 μm $\times$ 50 μm is about 130 nF cm^{-2}. The permittivity of sputtered Al_2O_3 thin film is estimated to be 8.14, which is about two times higher than that of SiO_2 deposited by LPCVD. After the gate dielectric deposition, sputtering of 300-nm-thick pure Al as gate electrode was performed, followed by gate patterning. Then a self-aligned boron implantation with a dose of 4×10^{15} cm^{-2} was done to form the source and drain. Then 500-nm-thick low-temperature oxide was deposited by LPCVD. Contact holes were opened and then sputtering of 700-nm-thick Al doped with 1% Si was performed, followed by electrode patterning. Finally, wafers were sintered in forming gas at 420 °C. The fabricated TFTs are named BG SPC TFT with Al_2O_3 gate dielectric. For comparison, another two kinds of TFTs were fabricated at the same time. One is conventional SPC poly-Si TFTs with 70-nm-thick-sputtered-Al_2O_3 gate dielectric, named SPC TFT with Al_2O_3 gate dielectric and the other is conventional SPC poly-Si TFT with 70-nm-thick-LPCVD-SiO_2 gate dielectric, named SPC TFT with SiO_2 gate dielectric. For all TFTs, after the fabrication, no further additional treatments are performed.

For characterization, the Agilent 4156A semiconductor parameter is used to test the device electrical performance. All TFTs used in this work have 24 μm in width (W) and 10 μm in length (L). The μ_{FE} is extracted from the following expressions [2],

$$\mu_{FE} = \frac{LdG_m}{W\varepsilon_{ox}V_{ds}}$$

$$G_m = \text{Max}\left(\frac{dI_{ds}}{dV_{gs}}\right)$$

where d, ε_{ox}, I_{ds} and G_m are physical gate dielectric thickness, gate dielectric permittivity, drain current and maximum of transconductance at $V_{ds} = -0.1$ V. The V_{th} is determined by the interception of linear extrapolation of a transfer curve at $V_{ds} = -0.1$ V. The *SS* is also extracted at $V_{ds} = -0.1$ V from the slope of log $|I_{on}|$ in the subthreshold region. The I_{on}/I_{off} ratio equals to maximum current over minimum current within the measured range. The *GIDL* current is defined at $V_{ds} = -5$ V and $V_{gs} = 5$ V.

3. Results and discussion

The transfer characteristic of SPC TFT with SiO_2 gate dielectric, SPC TFT with Al_2O_3 gate dielectric and BG SPC TFT with Al_2O_3 gate dielectric measured at $V_{ds} = -0.1$ and -5 V are shown in figure 3. The inset is log$|I_{on}|$ curves dependent on gate voltage plotted in subthreshold region for different devices. Compared to SPC TFT with SiO_2 gate dielectric (dark lines), all electrical parameters of SPC TFT with Al_2O_3 gate dielectric (red lines) are

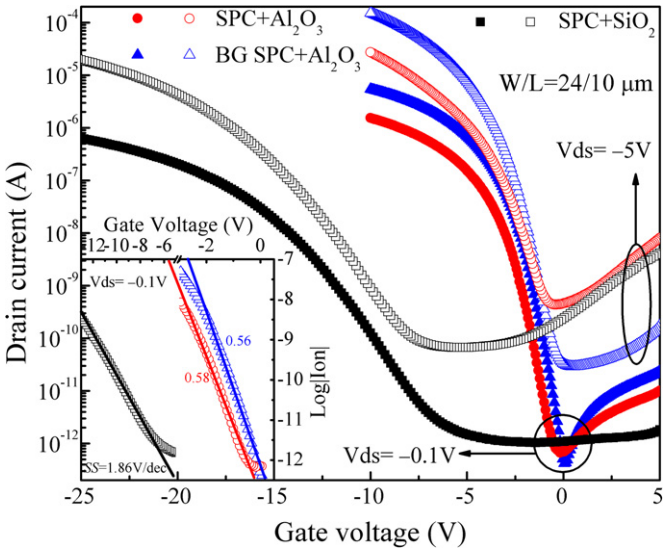

Figure 3. Transfer characteristics of SPC TFT with SiO_2 gate dielectric, SPC TFT with Al_2O_3 gate dielectric and BG SPC TFT with Al_2O_3 gate dielectric measured at $V_{ds} = -1$ and -5 V. The inset is log $|I_{on}|$ curves of subthreshold region for different devices.

improved, except *GIDL* current. By replacing SiO_2 dielectric with Al_2O_3 dielectric, the μ_{FE} increases from 8.74 to 16.67 cm^2 Vs^{-1}, the V_{th} reduces from -19.12 to -4.37 V and the *SS* decreases from 1.86 to 0.58 V dec^{-1}. However, the *GIDL* current increases from 4.20 to 8.09 nA. The related parameters are summarized in table 1. The thinner equivalent oxide thickness with the same physical thickness of high-k Al_2O_3 gate dielectric increases gate capacitance and improves the mobile carrier density, resulting in smaller V_{th} and *SS* [4–7]. Regarding the leakage mechanism of poly-Si TFTs [8–12], the I_{off} at high $|V_{ds}|$ is strongly dependent on the peak electric field E_p at the drain junction, which can be expressed by the following formulas,

$$I_{off} \propto \exp(\sqrt{E_p})$$

$$E_p = \frac{(V_{gs} - V_{ds} - V_{fb})\varepsilon_{ox}}{d\varepsilon_{Si}}$$

where ε_{Si} and V_{fb} are Si permittivity and flat-band voltage. Poly-Si TFT with high-k dielectric will bring larger E_p, giving rise to a rapid increase in off-state current.

To suppress this high off leakage current, BG active channel as described above is employed. As shown in figure 3, compared to SPC TFT with Al_2O_3 gate dielectric (red lines), the *GIDL* current of BG SPC TFT (blue lines) is greatly reduced by more than 43.9 times. For the BG SPC TFTs, a number of submicron-scale reverse-biased junctions are formed when the channel is in off-state region. The E_p near the drain junction can be partially distributed to the edge of BG lines [2], leading to reduced E_p and decreased *GIDL* current. Besides *GIDL* suppression, the μ_{FE}, V_{th}, *SS* and I_{on}/I_{off} ratio of BG SPC TFT with Al_2O_3 gate dielectric are also improved. The μ_{FE} is enhanced to 47.92 cm^2 Vs^{-1}, which is 1.8 times larger than that of SPC TFT with Al_2O_3 and 4.5 times larger than that of SPC TFT with SiO_2 gate dielectric. The V_{th} keeps decreasing to -3.85 V while the *SS* reduces a little, from

Table 1. Comparison of device parameters for different kinds of SPC TFTs at $|V_{ds}| = 0.1$ V.

Parameters	SPC TFT + 50 nm SiO_2 [7]	SPC TFT + SiO_2	SPC TFT + Al_2O_3	BG SPC TFT + Al_2O_3
μ_{FE} ($cm^2\ Vs^{-1}$)	11	8.74	16.67	47.92
$\|V_{th}\|$ (V)	12	19.12	4.37	3.85
SS (V dec^{-1})	2.06	1.86	0.58	0.56
I_{on}/I_{off}	4.65×10^6	6.13×10^5	2.31×10^6	1.30×10^7
I_{on}/I_{off} (@$V_{ds} = -5$ V)	–	2.93×10^5	6.23×10^4	5.24×10^6
GIDL (nA)	–	4.20	8.09	0.18

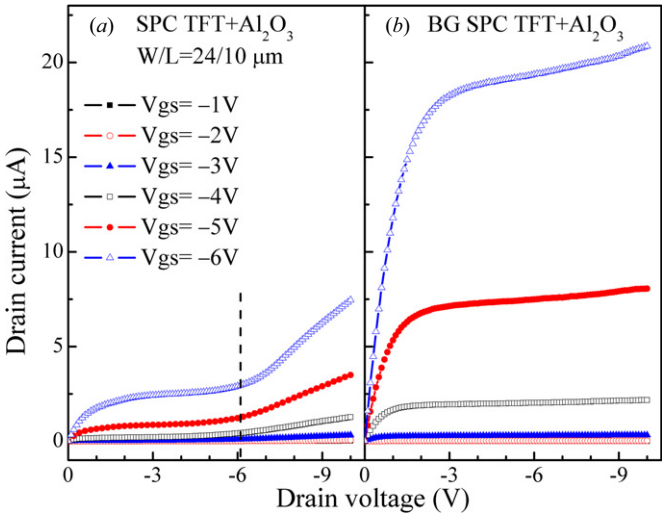

Figure 4. Output characteristics of (*a*) SPC TFT and (*b*) BG SPC TFT, measured at different V_{gs}.

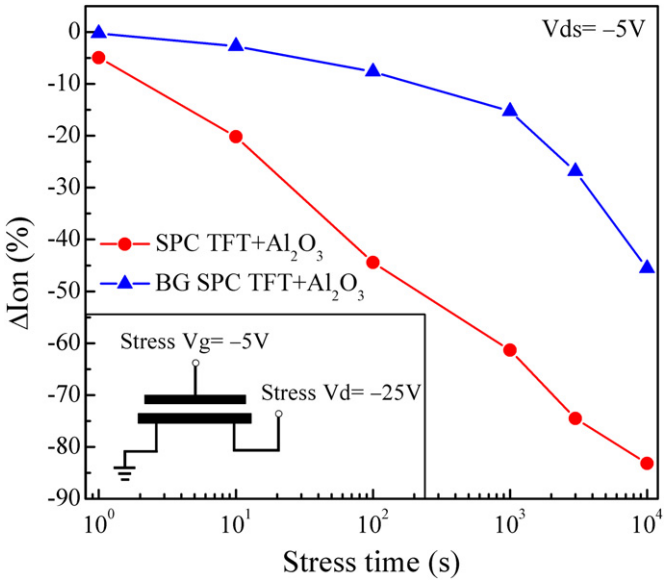

Figure 5. I_{on} degradation of BG SPC TFT with Al_2O_3 and SPC TFT with Al_2O_3 under HC stress. The inset is the stress condition.

0.58 to 0.56 V dec^{-1}. The I_{on}/I_{off} ratio of BG SPC TFT with Al_2O_3 gate dielectric at $V_{ds} = -0.1$ V is 1.3×10^7, which is 4.6 times larger than that of SPC TFT with Al_2O_3 gate dielectric and 20.2 times larger than that of SPC TFT with SiO_2 gate dielectric. The detailed parameter data are summarized in table 1. Compared to the SPC TFT with Al_2O_3 gate dielectric, the improved on-state characteristics of BG SPC TFT with Al_2O_3 gate dielectric is due to the BG lines, which links the grains, provides shortcuts for carriers and helps the carriers to find the more conductive path [2]. The output characteristics of SPC TFT with Al_2O_3 gate dielectric and BG SPC TFT with Al_2O_3 gate dielectric measured at different V_{gs} are shown in figures 4(*a*) and (*b*), respectively. The saturation current is greatly enhanced by more than four times, consistent to the transfer curve. It is also noted that for SPC TFT with Al_2O_3 gate dielectric the kink current can be clearly observed at $V_{ds} \approx -6$ V and $V_{gs} = -6$ V, while for BG SPC TFT with Al_2O_3 gate dielectric no kink current is observed at the same measurement range, implying the better hot carrier (HC) reliability of BG SPC TFT [13, 14]. To verify the better HC reliability of BG SPC TFT, HC stress test is performed on BG SPC TFT with Al_2O_3 and SPC TFT with Al_2O_3 as shown in figure 5. The stress condition is shown in the inset. It can be clearly observed that BG SPC TFT degenerates more slowly compared to normal SPC TFT at the same HC stress, consistent to kink effect suppression by BG structure in output curve.

4. Summary

High-performance SPC poly-Si TFTs with a high-*k* Al_2O_3 gate dielectric and BG active channel is demonstrated. The TFTs show outstanding electrical performance in terms of larger μ_{FE}, smaller V_{th}, steeper *SS* and larger I_{on}/I_{off} ratio compared to the control TFTs, which can satisfy the needs of peripheral driving circuit applications with low power and high speed.

Acknowledgment

This project was supported by Hong Kong Research Grants Council Theme Based Research Scheme Project No. T23-713/11-1.

References

[1] Ohshima H and Morozumi S 1989 *IEDM* p 157
[2] Zhou W, Meng Z, Zhao S, Zhang M, Chen R, Wong M and Kwok H S 2012 *IEEE Electron Device Lett.* **33** 1414
[3] Meng Z, Wang M and Wong M 2000 *IEEE Trans. Electron Devices* **47** 404
[4] Wilka G D, Wallace R M and Anthony J M 2001 *J. Appl. Phys.* **89** 5243

[5] Lin C P, Tsui B Y, Yang M J, Huang R H and Chien C H 2006 *IEEE Electron Device Lett.* **27** 360
[6] Chang C W, Deng C K, Huang J J, Chang H R and Lei T F 2008 *IEEE Electron Device Lett.* **29** 96
[7] Pan T M and Chang C J 2011 *Semicond. Sci. Technol.* **26** 075004
[8] Zhang M, Wang M, Lu X, Wong M and Kwok H S 2012 *IEEE Trans. Electron Devices* **59** 1730
[9] Yang M J, Chien C H, Lu Y H, Luo G L, Chiu S C, Lou C C and Huang T Y 2007 *IEEE Electron Device Lett.* **28** 902
[10] Yeh C F, Lin S S, Yang T Z, Chen C L and Yang Y C 1994 *IEEE Trans. Electron Devices* **41** 173
[11] Yazaki M, Takenaka S and Ohshima H 1992 *Japan. J. Appl. Phys.* **31** 206
[12] Hack M, Wu I W, King T J and Lewis A G 1993 *IEDM* p 385
[13] Koyanagi M, Kurino H, Hashimoto T, Mori H, Hata K, Hirumat Y, Fujimon T, Wu I W and Lewis A G 1991 *IEDM* p 571
[14] Zhang M, Wang M, Wang H and Zhou J 2009 *IEEE Trans. Electron Devices* **56** 2726